| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/856,212 | NAKAMURA ET AL. | |
| | Examiner | Art Unit | |
| | Matthew J. Song | 1722 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/27/2006*.

2. ☒ The allowed claim(s) is/are *9-13*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6/26/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

**EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Gerald Shekleton on 8/2/2006.

3. The application has been amended as follows:

- In Claim 9, A heat treating method ~~comprising~~ consisting of the steps of distributing oxide precipitates in a silicon single crystal wafer~~,~~ by a first step of maintaining a first heat treatment temperature for an initial entry of the silicon single crystal wafer up to 500°C, and a second step of maintaining a temperature ramping rate in a temperature range from the first heat treatment temperature to a second heat treatment temperature of 700°C-900°C, said ramping rate being 1°C/min or less, said first step being performed first after a wafer slicing process~~.~~, said wafer comprising a surface region of up to several tens of μm deep from a wafer surface and a bulk region of several tens or more of μm deep from the wafer surface, said wafer having been prepared from a crystal free from grown-in defects and produced by a Czochralski method, said oxide precipitates being uniformly distributed in the bulk region ~~by a first step of,. said heat treating method consisting of by a first step of maintaining a first heat treatment temperature for an initial entry of the silicon single crystal wafer up to 500°C, and a second step of maintaining a temperature ramping rate in a temperature range from the first heat treatment temperature to a second heat treatment temperature of 700°C-900°C, said ramping rate being 1°C/min or less, said first step being performed first after a wafer slicing process~~.

- In Claim 10, A heat treating method ~~comprising~~ consisting of the steps of distributing oxide precipitates in a silicon single crystal wafer, by a first step of maintaining a first heat treatment temperature for an initial entry of the silicon single crystal wafer up to said 500°C, and a second step of maintaining a temperature ramping rate in a temperature range from the first heat treatment temperature to a second heat treatment temperature of 700°C-900°C, said ramping rate being 1°C/min or less, so as to make uniform the distribution of an oxide precipitate density of the silicon single crystal wafer in the wafer, said first step being performed first after a wafer slicing process, said wafer comprising a surface region of up to several tens of μm deep from a wafer surface and a bulk region of several tens or more of μm deep from the wafer surface, said wafer having been prepared from a crystal free from grown-in defects and produced by a Czochralski method, said oxide precipitates being uniformly distributed in the bulk region ~~said heat treating method consisting of.~~ ~~by a first step of maintaining a first heat treatment temperature for an initial entry of the silicon single crystal wafer up to 500°C, and a second step of maintaining a temperature ramping rate in a temperature range from the first heat treatment temperature to a second heat treatment temperature of 700°C-900°C, said ramping rate being 1C/min or less, so as to make uniform the distribution of an oxide precipitate density of the silicon single crystal wafer in the wafer, said first step being performed first after a wafer slicing process.~~

- In Claim 11, A heat treating method consisting of the steps of distributing oxide precipitates in a silicon single crystal wafer, by a first step of controlling a first heat treatment temperature for an initial entry of the silicon single crystal wafer to be a target of the heat treatment and a second step of controlling a temperature ramping rate from the heat treatment temperature in initial entry to a higher second heat treatment temperature and maintaining in a range of 700°C-900°C so as to make the distribution of an oxide precipitate density of the silicon single crystal wafer more uniform after heat treatment, said first step being performed first after a wafer slicing process. said wafer comprising a surface region of up to several tens of μm deep from a wafer surface and a bulk region of several tens or more of μm deep from the wafer surface, said wafer having been prepared from a crystal free from grown-in defects and produced by a Czochralski method, said oxide precipitates being uniformly distributed in the bulk region ~~consisting essentially~~

~~of the central region by a first step of~~. ~~said heat treating method consisting of by a first step of controlling a first heat treatment temperature for an initial entry of the silicon single crystal wafer to be a target of the heat treatment and a second step of controlling a temperature ramping rate from the heat treatment temperature at initial entry to a higher second heat treatment temperature and maintaining in a range of 700°C-900°C so as to make the distribution of an oxide precipitate density of the silicon single crystal wafer more uniform after heat treatment, said first step being performed first after a wafer slicing process.~~

***Allowable Subject Matter***

4. Claims 9-13 are allowed.

5. The following is an examiner's statement of reasons for allowance: The closest prior art Furuya et al (JP 6-97179) and Bischoff et al (US 4,437,922). Furuya et al and Bischoff et al teaches heat treatment processes which comprise a first step of maintaining a temperature from an initial entry temperature to 500°C and a second step of increasing temperature at a rate of less than 1°C/min up to a temperature of 900°C ('922 Fig 2 and '179 Abstract). Furuya et al and Bischoff et al teaches additional heat treatment steps. Furuya et al and Bischoff et al does not teach or suggest a heat treatment process which only consists of the claimed first and second step.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on 571-272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew J Song
Examiner
Art Unit 1722

MJS
August 9, 2006

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